REMARKS

Claims 9, 25, 28 and 48 have been amended. Claims 14-19, 33-39 and 55-62 have been withdrawn. No claims have been cancelled and no new claims have been added. No new matter has been added. Claims 1-13, 20-32 and 40-54 are pending.

Disclaimers Relating to Claim Interpretation and Prosecution History Estoppel

Claims 9, 25, 28 and 48 have been amended notwithstanding the belief that these claims were allowable. Except as specifically admitted below, no claim elements have been narrowed. Rather, cosmetic amendments have been made to the claims and to broaden them. Claims 9, 25, 28 and 48 have been amended solely for the purpose of expediting the patent application process, and the amendments were not necessary for patentability.

The claims of this application are intended to stand on their own and are not to be read in light of the prosecution history of any related or unrelated patent or patent application. Furthermore, no arguments in any prosecution history relate to any claim in this application, except for arguments specifically directed to the claim.

Election/Restrictions

The Examiner required restriction to either Group I (claims 1-13, 20-32, 40-54) or Group II (claims 14-19, 33-39, 55-62). Group I is hereby elected without traverse. The Group II claims are hereby withdrawn.

Information Disclosure Statements

An Information Disclosure Statement (IDS) has been filed in this Application. The Examiner has not examined two of the references cited in the IDS because publication dates were not provided, namely "PowerQuest, Partitioning White Paper for Partition Magic" and "PowerQuest product description for Partition magic 8.0". A new IDS is being filed concurrently herewith.

Claim Rejections - 35 USC § 112

The Examiner rejected claims 9, 25, 28 and 48 under 35 USC § 112, second paragraph as being indefinite. This rejection is respectfully traversed.

Cosmetic amendments have been made to claims 9, 25, 28 and 48 reciting that the offset is obtained from the virtual device table. These amendments have been made solely to advance prosecution of this matter and were not necessary for compliance with 35 USC § 112. In view of these amendments the 35 USC § 112 rejection is moot and should be withdrawn.

Claim Rejections - 35 USC § 102

The Examiner rejected claims 1, 4, 5, 10, 20, 22-23, 29, 40, 43, 44, 49, 53 and 54 under 35 USC § 102(b) as anticipated by Fukunaga (US 4481573). This rejection is respectfully traversed. Of this group of rejected claims, claims 1, 20 and 40 are independent.

Fukunaga appears to be wrongly cited and appears to not be applicable to the claims listed in this rejection. In the entirety of Fukunaga, the term "hard disk" is not used.

The Office action directs us to portions of Fukunaga that describe a prior art system in which a least recently used technique for access between a main memory and an external memory is taught. Specifically, the cited portions in col. 1 of Fukunaga recite

> A data processing system in which a main memory is shared by a plurality of processors is generally called a multiprocessor system. One of the problems to be resolved in the multiprocessing system is a virtual memory system. The virtual memory system has been known well (for example, by U.S. Pat. No. 3,829,840 issued on Aug. 13, 1974). In the virtual memory system, a main memory and an external memory are regarded to be apparently integral, and when information requested by a processor is not in the main memory but in the external memory, the system automatically transfers a portion of information in the main memory which is less frequently used to the external memory and transfers the requested information from the external memory to the main memory.
>
> Fukunaga, 1:18-26

As to the teachings of Fukunaga, the cited portion of col. 6 describes a technique for memory access upon the occurrence of an instruction being absent from a cache. Specifically, the cited portion of Fukunaga recites

> When the I unit 43 fetches an instruction word to be executed, the presence or absence of the instruction word on the instruction cache 41 is checked, and if it is present the data is transferred to the I unit 43 as the instruction word through the bus 45. If it is absent, a virtual address of the instruction word is transferred to the memory control unit 12 through the common bus 50.
>
> The memory control unit 12 translates the virtual address to the physical address to access the main memory 10 through the memory bus 11. The accessed data (instruction) is sent to the instruction cache 41 through the common bus 50 and to the I unit 43 through the bus 45, is processed in the I unit 43 and stored in the instruction cache 41.
>
> Fukunaga, 6:44-58

The Office action asserts that the memory control unit 12, the common bus 50, the memory bus 11 in co. 6 when combined with the prior art discussion of col. 1 teach all of the limitations recited in the independent claims. However, the teachings of the cited portions of Fukunaga fail to in any way teach the limitations recited in the claims.

In contrast to the teachings of Fukunaga, claim 1 is directed to "A method for sharing a hard disk among multiple users of a computer" claim 20 is directed to "A sharing device to be coupled with a computing device having a hard disk". Though reciting various features, claims 1 and 20 both recite "a hard disk", "a hard disk access command" and "a hard disk address". There is no teaching in Fukunaga of "a hard disk", "sharing a hard disk", "a hard disk access command" and "a hard disk address". As to claim 40, claim 40 is directed to "A method for sharing a storage device among multiple users of a computing device". The teachings of Fukunaga fail to describe the claimed "method for sharing a storage device among multiple users of a computing device." Further, Fukunaga fails to teach the receiving, the translating and the forwarding steps recited in each of the independent claims. As such, the cited portions of Fukunaga and the entirety of Fukunaga appears to be wholly inapplicable to the independent claims.

In addition, the Office action cites a portion of Fukunaga that states that "A data processing system in which a main memory is shared by a plurality of processors is generally called a multiprocessor system." (Fukunaga, 1:18-20) The relevance of this teaching is not understood. There is not mention of a "multiprocessor system" in the pending patent application or in the claims. Please provide clarification.

For all of the reasons set forth above, Fukunaga both fails to teach each and every one of the limitations recited in the independent claims and fails to teach the limitations for which it is cited. As such claims 1, 20 and 40 are patentable over Fukunaga. Further, all claims which depend on claims 1, 20 and 40, including claims 4, 5, 10, 22, 23, 29, 43, 44, 49, 53 and 54, are patentable over Fukunaga. Therefore, this rejection should be withdrawn.

Claim Rejections - 35 USC § 103

A. Rejections based on Fukunaga and Aguilar

The Examiner rejected claims 2, 7, 21, 26, 41 and 46 under 35 USC § 103(a) as obvious from Fukunaga in view of Aguilar (US 6799316). This rejection is respectfully traversed. Aguilar fails to cure the deficiencies of Fukunaga asserted above. As such, all of the limitations recited in claims 2, 7, 21, 26, 41 and 46 are not taught by the combination of cited references. Therefore, claims 2, 7, 21, 26, 41 and 46 are patentable over the cited references and this rejection should be withdrawn.

Moreover, even if *in arguendo* Fukunaga taught or suggested the limitations for which it is asserted (and it does not), Aguilar fails to teach or suggest the limitations for which it is cited. Aguilar teaches a system for intercepting legacy hardware instructions. As taught in the portion of Aguilar cited in the Office action, when "The memory address does not match a memory location of a legacy device the process ends." (Aguilar, 8:3-6) When the memory address "does match a virtual hardware device, the corresponding IO instruction on the data bus is intercepted or hooked (step 508)." (Aguilar, 8:6-10) As such, Aguilar does not teach or suggest the mapping features recited in 2, 7, 21, 26, 41 and 46. Further, Aguilar fails to teach or suggest the mapping features in the context of any of "A method for sharing a hard disk among multiple users of a computer" as recited in claims 2 and 7, "A sharing device to be coupled with a computing device having a hard disk" as recited in

claims 21 and 26, and "A method for sharing a storage device among multiple users of a computing device" as recited in claims 41 and 46. As such, all of the limitations recited in claims 2, 7, 21, 26, 41 and 46 are not taught by the combination of cited references. Therefore, claims 2, 7, 21, 26, 41 and 46 are patentable over the cited references and this rejection should be withdrawn.

B. Rejections based on Fukunaga, Aguilar and Hsu

The Examiner rejected claims 3 and 42 under 35 USC § 103(a) as obvious from Fukunaga in view of Aguilar and Hsu (US 5526504). This rejection is respectfully traversed. Hsu fails to cure the deficiencies of Fukunaga and Aguilar asserted above. As such, all of the limitations recited in claims 3 and 42 are not taught by the combination of cited references. Therefore, claims 3 and 42 are patentable over the cited references and this rejection should be withdrawn.

C. Rejections based on Fukunaga, Aguilar and Porterfield

The Examiner rejected claims 8, 9, 27, 28, 47 and 48 under 35 USC § 103(a) as obvious from Fukunaga in view of Aguilar and Porterfield (US 6418523). This rejection is respectfully traversed. Porterfield fails to cure the deficiencies of Fukunaga and Aguilar asserted above. As such, all of the limitations recited in claims 8, 9, 27, 28, 47 and 48 are not taught by the combination of cited references. Therefore, claims 8, 9, 27, 28, 47 and 48 are patentable over the cited references and this rejection should be withdrawn.

D. Rejections based on Fukunaga and Porterfield

The Examiner rejected claims 6, 11-13, 24, 25, 30-32, 45 and 50-52 under 35 USC § 103(a) as obvious from Fukunaga in view of Porterfield. This rejection is respectfully traversed. Porterfield fails to cure the deficiencies of Fukunaga asserted above. As such, all of the limitations recited in claims 6, 11-13, 24, 25, 30-32, 45 and 50-52 are not taught by the combination of cited references. Therefore, claims 6, 11-13, 24, 25, 30-32, 45 and 50-52 are patentable over the cited references and this rejection should be withdrawn.

Conclusion

It is submitted that the independent and dependent claims include other significant and substantial recitations which are not disclosed in the cited references. Thus, the claims are also patentable for additional reasons. However, for economy the additional grounds for patentability are not set forth here.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited.

The Examiner is invited to call the undersigned registered practitioner to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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